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Title

PARTITIONING OF SPECIAL CIRCUITS

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ABSTRACT:

In this paper, partitioning of special type of circuit and short circuit testing have been discussed. Some theoretical explanations have also been established.

Key words: Graph, Partitioning of Circuits, Lshape Floor Plane.

INTRODUCTION:

The importance of graph theory has been rising up since the application of them in computer science, electronics and telecommunication technology and other branches of science too. There are many applications of graph in the above cited branches of science and technology. They are, namely interval graph, hyper graph, crossing number of graphs, dual graphs, triangulated graphs which have many important application in VLSI design technology. The thickness and crossings of non-planar graph play an important role in VLSI design. The partitioning of graph/ circuit is also another important section of CAD technology. A new structure of a circuit such that G($2m+2$, $2m^2+3m$) for $m \geq 2$ [1] has been found, where m is the number of modules. This type of circuit can be obtained for $2n+3$ number of nets for $n \geq 1$ with simultaneous changes of $m \geq 2$. The following circuit [figure-1] is shown for m=2 and n=1.

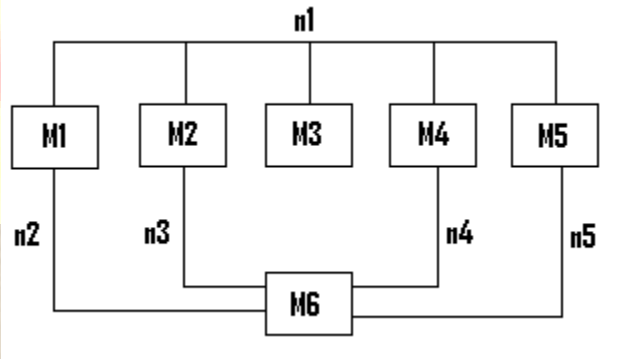

Figure-1

Again it has been focused by kalita [1] that the above circuit/ graph obtained for m≥2 for the number of modules and for n≥1 for the number of nets is a non-planar graph which helps to study the lower bound of crossings of non-planar graphs. It has also been discussed that a circuit of the form K(2m+2,6m) for m ≥2 can be obtained from the circuit G(2m+2,2m^2+3m) for m ≥2 and the circuit K (2m+2, 6m) for m ≥2 will give a special type of floor plan and this graph is planar. An important algorithm has been developed by Kalita (2009) to find out the graphs from hyper graphs. Various properties have been found relating to elimination of complex triangle from the circuit G (2m+2, 2m^2+3m) for m ≥2 ,existence of 1-uniform, 2-uniform, 3-uniform hyper graphs etc. It has also been forwarded by various authors [7-11] the application of some special type of graphs in VLSI design. The most important part of VLSI design technology is circuit partitioning and it has been found that the circuit is considered as a graph or hyper graph. Again, the CAD designer has been discussed the crossings number of a graph, when they design the printed circuit board. Hence the minimum number of crossings of non-planar graphs has been playing the very important role since existence of VLSI design technology. The crossings and thickness of special type of graphs has been discussed by Kalita . etal [2007]. Some results, regarding the thickness and crossings and edge-disjoint Hamiltonian Circuit of non-planar graphs G$'$(2m+2,6m+2) and H$'$ (2m+3,6m+8) for m ≥2 have been discussed by Kalita etal [2007]. Besides, the construction of line graphs L(H) and L(G) of the graphs H(2m+2,6m) and G(2m+3,6m+3) for m ≥2 with some properties have also been found respectively by Kalita . etal [2008]. In 2005, Kalita has also been forwarded some important properties of non-planar graphs. Some theoretical aspects regarding the thickness and Hamiltonian circuit have also been forwarded there. Recently Kalita.etal [2009] has been developed the most important properties of graphical partitions related with some graphs. There are some important unsolved problems of circuit partitioning of graphs and hyper graphs and short circuit existence between any two net pattern for printed circuit board . An algorithm to obtain a graph from hyper graphs has been forwarded by Kalita [2009]. The approach of testing printed circuit board for the existence of possible short circuit is an important problem in VLSI design technology. It is known that one can construct a graph ,which is known as a line of sight graph that has a vertex corresponding to each net and where two vertices are joined by an edge if and only if there could be a short circuit between the corresponding net. Again, it is known that a good procedure is to partition the set of

nets into subsets such that if the two nets are in the same subsets, then there does not have a short between them.

In this paper, we are going to focus theoretical relationship of graph/circuit where a short circuit exist when designed a printed circuit board during manufacturing process. In addition to this, we have been discussed the acceptability condition of a particular circuit partitioning problem.

Theorem [1]: Let G (2m+2,6m) for m ≥2 be a circuit where 2m+2 for m ≥2 is the number of nets and the number of grid points is $(2m+2)^2$. Then there will be four partition and the comparison for short circuit is equal to the number of edges of the complete graph K_{2m+2} for m ≥2 and possible test is equal to 4.

Proof: It has been found that any planar graph is a line of sight graph for some pattern of grid segments of a circuit. Here, the graph / circuit G (2m+2,6m) for m ≥2 is a planar graph and it has been known that this graph is four colorable. Hence there are four partitions [6].The following figures (Figure-2 and Figure-3) give a grid points and line of sight graph for m=2.

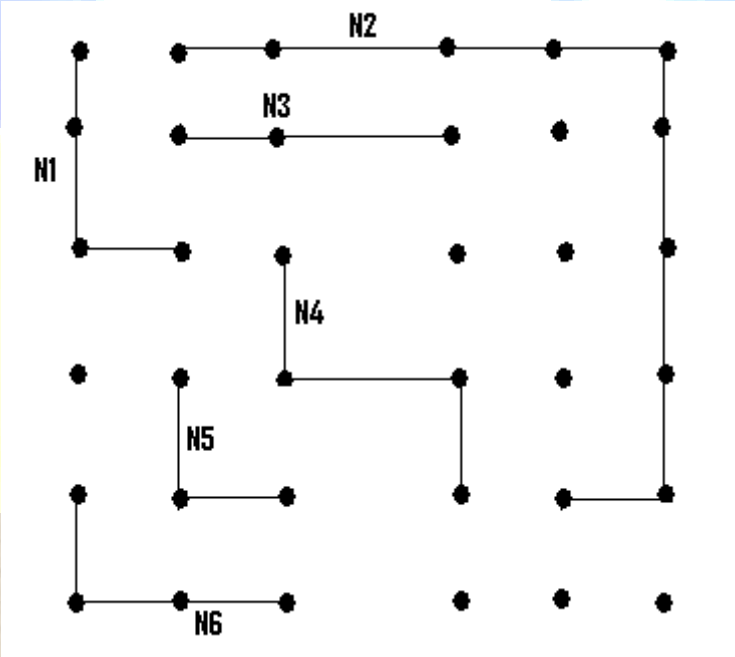

Figure-2

A grid of 36 nodes and six nets comprising altogether 22 grid segments.

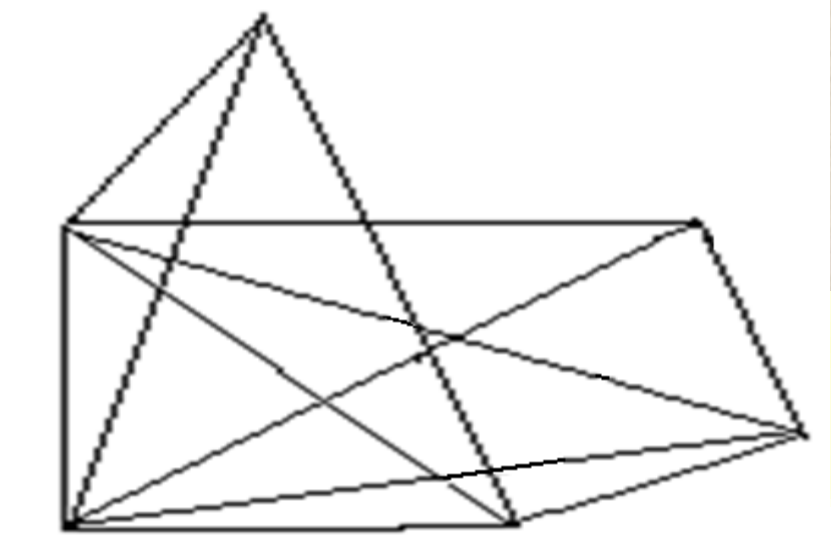

Figure-3

Line of sight graph of six vertices.

The number of comparison for short circuit of Figure-2 is C^6_2 =15 and this is equal to the number of edges of the complete graph K_6 . Now , applying the same calculation of comparison for the short circuit of 2m+2 nets and $(2m+2)^2 = 4m^2 + 8m + 4$ nodes we have $2m^2+3m+1$ the number of comparison for m ≥2 which is equal to the number of edges of the complete graph K_{2m+2} for m ≥2. Again it is clear that the line of sight graph (figure-3) is four colorable and hence exactly there is 4 possible test needed.

Theorem[2]: If the vertex set of a circuit G(2m+2, 6m) for m ≥2 is partitioned into 2≤ r ≤2m+1 for m ≥2 , where r is the number of partitions , then the partition is acceptable if the weight of the vertices are equal to unity.

Proof: We prove the theorem in various cases.

Case1: If there exist only two partitions having same number of vertices in the graph/ circuit, (r=2), when m=2 ,then the result is true. Suppose, N_1= { V_1, V_2, V_3 }

N_2={ V_4, V_5, V_6 } be two partitions. Since the weights of each vertex is equal to unity , hence immediately it satisfies the condition of acceptability $b(i) \leq w(N_i) \leq B(i)$, where $w(N_i)$ is the sum of weight of the vertices in N_i , B(i) is the maximum size of part i and b(i) is the minimum size of part i [7] .

Continuing the process if the set N_1 contains two vertices and N_2 contains four vertices or if N_1 contains one vertex and N_2 contains five vertices then also the condition of acceptability is satisfied.

Case2: If there exist three partitions (r=3) or four partitions (r=4) or five partitions (r=5) ……then also the condition of acceptability above is satisfied as the weight of the vertices of the circuit equal to unity.

We now suppose without loss of generality the result is true for r=2m+1 for m ≥2.

Let the result be true for m=k≥2. Hence the result is true for r=2k+1. The result for m=k+1 implies that r=2(k+1) +1 =2k+2+1=2k+3.

We know that our result is related with the values of m ≥ 2, hence

m ≥ 2 implies k+1 ≥ 2 implies k ≥ 1 which shows that r=2k+3≥2 implies k ≥1. Hence for all values of k ≥1 that is for m ≥2 the partition

$2 \leq r \leq 2m+1$ is acceptable for the given circuit. Hence the proof..

Theorem[3]: The bipartition of the circuit G (2m+2,6m) for m ≥2 is acceptable if the weights of the vertices are three each and if one partition contain one vertex and the other contain 2n+3 vertices for n ≥1 with simultaneous changes of m ≥2.

Proof: We prove the theorem by induction method. Here , we have the total number of weights is 3(2m+2)=6m+6 for m ≥2 , as the weights of the vertices are three each. Hence when bipartition say N1 and N2 exists then according to our statement of the theorem N1 contain one vertex and N2 contains 2n+3 vertices for n ≥1 and hence the condition of acceptability $b(i) \leq w(N_i) \leq B(i)$ is satisfied for the two partitions N1and N2 as discussed in the theorem 2 above. [for m=2, we have $1 \leq 3 \leq 5$.] Hence for m=2 and n=1, the result is true.

Now let the theorem be true for m=L ≥2 and n=k.

Then we have that one partition N1 contains one vertex and other partition N2 contains 2k+3 for k≥1.Now if we put n=k+1 and m= L+1 ≥2, then we have the partition N1 contains one vertex and the other partition N2 contains 2(k+1) +3 = 2k+5 vertices.

It is clear that m=L+1 ≥ 2 implies L ≥ 1 and

n= 2k+5 ≥ 1 implies 2k ≥ -4

implies k ≥ -2, which shows that the result is true. This completes the proof.

Corollary: The bipartition (r=2) of the circuit G(2m+2, 6m) for m ≥ 2 is acceptable if the weights of the vertices are two each and one partition contain two vertices and other contains 2n+2 vertices for n ≥ 1.

Proof: Same as theorem 3.

Remarks: The graphs / circuits discussed in theorems 1, 2 and 3 always gives l shaped floor plane and which will be discussed in near future.

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